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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,334	05/31/2006	Yaozu Dong	42P22613	6239
59796 7590 12/22/2010				
INTEL CORPORATION c/o CPA Global P.O. BOX 52050 MINNEAPOLIS, MN 55402			EXAMINER KESSLER, GREGORY AARON	
			ART UNIT 2196	PAPER NUMBER
			NOTIFICATION DATE 12/22/2010	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

heather.ladamson@intel.com

# Office Action Summary

**Application No.**

10/581,334

**Applicant(s)**

DONG, YAOZU

**Examiner**

GREGORY A. KESSLER

**Art Unit**

2196

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 October 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 August 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-040)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB-08)  
Paper No(s)/Mail Date 12/02/2010
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. Claims 1-27 are presented for examination. Claims 1, 10, 11, and 20 are amended.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 6, 10-12, 16, 20, 21, 25, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinechin et al (**U.S. Pat. Pub. No. 2006/0026385 A1, hereinafter Dinechin**) in view of Traut (**U.S. Pat. No. 7210144 B2**).

Dinechin was cited in the previous office action.

3. As per claim 1, Dinechin teaches the limitations as claimed, including a method for supporting virtual machines in a data processing system, the method comprising:  
executing an emulation patch for a guest virtual machine (VM) of a processing system, the emulation patch including data to facilitate identification of a routine for emulating a guest instruction (Paragraph [0028], Lines 7-12; Paragraph [0052], Lines 1-17);

in response to execution of the emulation patch, transferring control from the guest VM to a virtual machine monitor (VMM) (Paragraph [0052], Lines 12-17; Figure 15 shows a branch instruction transferring control from the virtual machine to the virtual machine monitor); and

using the data from the emulation patch to find an emulation routine for the guest instruction (Paragraph [0052], Lines 12-17; Paragraph [0028], Lines 7-12; Figure 15, Element 1504 shows using the data from the patch to find an emulation routine, Element 1502).

Dinechin does not expressly teach that the steps of the method are performed without saving contextual data that defines a system state for the guest VM.

However, Traut teaches that the steps of the method are performed without saving contextual data that defines a system state for the guest VM (Col. 5, Lines 47-54 and Figure 2, Elements 220 and 222 teach patching a guest instruction in a virtual machine without saving any of the system state of the virtual machine as it existed prior to patching).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Traut with those of Dinechin in order to allow for Dinechin's method to more efficiently execute the patching steps by not requiring the further overhead of saving system state information along with the patching process.

4. As per claim 2, Dinechin teaches that the operation of executing an emulation patch comprises executing an instruction that includes an immediate value to be used for finding the emulation routine (Figure 15, Element 1504).
5. As per claim 6, Dinechin teaches automatically determining whether the guest instruction is to be patched for emulation, based at least in part on a list of instructions to be patched (Paragraph [0055], Lines 18-22; Paragraph [0056], Lines 1-3) and inserting the emulation patch in response to a determination that the guest instruction is to be patched (Paragraph [0056], Lines 6-10).
6. As per claim 10, Dinechin teaches in response to execution of the emulation patch, finding and executing the emulation routine for the guest instruction without decoding the guest instruction (Paragraph [0052], Lines 12-17 teach finding and executing the emulation routine with no mention of decoding the guest instruction; Figure 15).
7. As per claims 11, 12, and 16, they are processing system claims of method claims 1, 2, and 6, respectively. Therefore, they are rejected for the same reasons.
8. As per claims 20, 21, 25, and 27, they are apparatus claims of method claims 1, 2, 6, and 10, respectively. Therefore, they are rejected for the same reasons.

9. Claims 3, 4, 13, 14, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinechin and Traut, as applied to claim 1 above, and further in view of Gates (**U.S. Pat. No. 6449709 B1**).

Gates was cited in the previous office action.

10. As per claim 3, Dinechin teaches that the operation of executing an emulation patch comprises executing a flow control instruction, wherein the flow control instruction includes an address to be used for finding the emulation routine, the flow control instruction selected from a group consisting of a branch instruction (Figure 15, Element 1504; Paragraph [0028], Lines 7-12).

Dinechin and Traut do not teach a call instruction or a jump instruction.

However, Gates teaches a call instruction and a jump instruction (Col. 10, Lines 21-34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Gates with those of Dinechin and Traut in order to allow for more flexibility in the selection of the flow control instruction to provide for situations where a different known instruction, such as a call or a jump instruction, would be more appropriate.

11. As per claim 4, Dinechin teaches that the operation of executing an emulation patch comprises executing an instruction selected from the group consisting of a branch instruction (Figure 15, Element 1504; Paragraph [0028], Lines 7-12).

Dinechin and Traut do not teach a break instruction, a call instruction, or a jump instruction.

However, Gates teaches a break instruction, a call instruction, and a jump instruction (Col. 10, Lines 21-34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Gates with those of Dinechin and Traut in order to allow for more flexibility in the selection of the flow control instruction to provide for situations where a different known instruction, such as a break, call, or jump instruction, would be more appropriate.

12. As per claims 13 and 14, they are processing system claims of method claims 3 and 4, respectively. Therefore, they are rejected for the same reasons.

13. As per claims 22 and 23, they are apparatus claims of method claims 3 and 4, respectively. Therefore, they are rejected for the same reasons.

14. Claims 5, 7-9, 15, 17-19, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinechin and Traut, as applied to claim 1 above, and further in view of Dinechin et al (**U.S. Pat. Pub. No. 2006/0026387 A1, hereinafter Dinechin2**).

Dinechin2 was cited in the previous office action.

15. As per claim 5, Dinechin and Traut do not expressly teach determining an index, based at least in part on data produced by the emulation patch and using the index to find the emulation routine to be executed.

However, Dinechin2 teaches determining an index, based at least in part on data produced by the emulation patch and using the index to find the emulation routine to be executed (Paragraph [0055], Lines 19-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Dinechin2 with those of Dinechin and Traut in order to take advantage of a variety of known methods for transferring control from the virtual machine to the virtual machine monitor using the emulation patch.

16. As per claim 7, Dinechin teaches automatically determining whether the guest instruction is to be patched for emulation, based at least in part on a list of instructions to be patched (Paragraph [0055], Lines 18-22; Paragraph [0056], Lines 1-3).

Dinechin and Traut do not teach retrieving a code template that corresponds to the guest instruction to be patched.

However, Dinechin2 teaches retrieving a code template that corresponds to the guest instruction to be patched (Paragraph [0069], Lines 17-24).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Dinechin2 with those of Dinechin and Traut in order to take advantage of a variety of known methods for transferring control from the virtual machine to the virtual machine monitor using the emulation patch.

17. As per claim 8, Dinechin teaches automatically determining whether the guest instruction is to be patched for emulation, based at least in part on a list of instructions to be patched (Paragraph [0055], Lines 18-22; Paragraph [0056], Lines 1-3).

Dinechin and Traut do not teach retrieving a code template that corresponds to the guest instruction to be patched and generating the emulation routine for emulating the guest instruction, based at least in part on the code template.

However, Dinechin2 teaches retrieving a code template that corresponds to the guest instruction to be patched and generating the emulation routine for emulating the

guest instruction, based at least in part on the code template (Paragraph [0069], Lines 17-24).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Dinechin2 with those of Dinechin and Traut in order to take advantage of a variety of known methods for transferring control from the virtual machine to the virtual machine monitor using the emulation patch.

18. As per claim 9, Dinechin teaches automatically determining whether the guest instruction is to be patched for emulation, based at least in part on a list of instructions to be patched (Paragraph [0055], Lines 18-22; Paragraph [0056], Lines 1-3), wherein the guest instruction resides in a slot of an instruction bundle (Paragraph [0049], Lines 1-6).

Dinechin and Traut do not teach retrieving a code template that corresponds to the guest instruction to be patched and generating the emulation routine for emulating the guest instruction, based at least in part on the code template and on the slot containing the guest instruction.

However, Dinechin2 teaches retrieving a code template that corresponds to the guest instruction to be patched and generating the emulation routine for emulating the

guest instruction, based at least in part on the code template and on the slot containing the guest instruction (Paragraph [0069], Lines 17-24).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Dinechin2 with those of Dinechin and Traut in order to take advantage of a variety of known methods for transferring control from the virtual machine to the virtual machine monitor using the emulation patch.

19. As per claims 15, 17, 18, and 19, they are processing system claims of method claims 5, 7, 8, and 9, respectively. Therefore, they are rejected for the same reasons.

20. As per claims 24 and 26, they are apparatus claims of method claim 5 and 8, respectively. Therefore, they are rejected for the same reasons.

### ***Response to Arguments***

21. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GREGORY A. KESSLER whose telephone number is (571)270-7762. The examiner can normally be reached on Monday - Friday, 7:30 a.m. - 5:00 p.m., alternate Fridays, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emerson Puente can be reached on (571)272-3652. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/GREGORY A KESSLER/  
Examiner, Art Unit 2196

/Emerson C Puente/  
Supervisory Patent Examiner, Art Unit 2196